REMARKS

Applicants respectfully request the Examiner's reconsideration of the present application.

Applicants would like to thank the Examiner for discussing the claim rejections under 35 U.S.C. § 101 over the phone on July 25, 2008 and for providing suggestions on claim amendments on how to overcome the rejections.

Claims 1, 3, and 5-22 in the present application are pending.

Claims 1, 3, and 5-22 are rejected under 35 U.S.C. § 101.

Claims 1, 3, 5-7, 9, and 11-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,711,602 ("Bhandal") in view of U.S. Patent No. 7,046,723 ("Schier").

Claims 1, 11, 17, 21, and 22 have been amended. Support for the amendment to claims may be found in paragraphs [0005] and [0028]-[0047], Figures 2-5, and claims 1-20 as originally filed. No new matter has been added.

Claims 1-3, and 5-22 are rejected under 35 U.S.C. § 101.

In the Advisory Action mailed 7/16/2008, the Office states in part that

> In addition, the alleged feature of producing a summing scaled product of the input operands without having to employ a DSP capable of multiplying at least the total number of bits of the two numbers is not explicitly or directly seen in the claims.

(7/16/2008 Advisory Action, p. 2).

Applicants submit that claim 1 has been amended to include the limitation "performing multiplication of a first number with a second number on a field programmable gate array without utilizing a digital signal processor (DSP) capable of multiplying a number of bits forming the first and second numbers" in the preamble as suggested by the Examiner. Claims 11, 17, 21, and 22 have been amended to include similar limitations.

Applicants submit that in view of the amendments, claims 1-3, and 5-22 more clearly describe a practical application to produce a "useful, concrete, and tangible result", i.e., the value representing a product of the first and second number, wherein the first and second number each have a number of bits equal to or greater than the total of the first and second number of bits. By virtue of the method of Claim 1, the product of the first and second numbers can be obtained by the field programmable gate array despite the fact that the DSP of the field programmable array is capable of multiplying only a fewer number of bits than those forming the two numbers. As such, the result of the method clearly is "useful, concrete, and tangible" in that it is achieved without having to utilize a DSP capable of multiplying a number of bits forming the two numbers.

Applicants submit that in view of the amendments to claims 1, 11, 17, 21, and 22, claims 1-3, and 5-22 are patentable under 35 U.S.C. §101.

Claims 1, 3, 5-7, 9, and 11-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over 6,711,602 ("Bhandal") in view of U.S. Patent 7,046,723 ("Schier").

It is submitted that Bhandal and Schier do not render claims 1, 3, 5-7, 9, and 11-22 unpatentable under 35 U.S.C. §103(a).

Bhandal includes a disclosure of a pair of parallel 16.times.16 multipliers each with two 32-bit inputs and one 32-bit output. There are options to allow input halfword and byte selection for four independent 8x8 or two independent 16x16 multiplications, real and imaginary parts of complex multiplication, pairs of partial sums for 32x32 multiplication, and partial sums for 16x32 multiplication. There are options to allow internal hardwired routing of each multiplier unit results to achieve partial-sum shifting as required to support above options. There is a redundant digit arithmetic adder before final outputs to support additions for partial sum accumulation, complex multiplication vector accumulation and general accumulation for FIRs/IIRs--giving MAC unit functionality. There are options controlled using bit fields in a

control register passed to the multiplier unit as an operand. There are also options to generate all of the products needed for complex multiplication (see Bhandal Abstract).

Schier includes a disclosure of a digital and a multiplication method are described, which lead to an efficient architecture for a hardware implementation of digital FIR and IIR filters into FPGAs. The multiplications of input sample data and delayed sample data with filter coefficients are performed by addressing look-up tables in which corresponding multiplication results are prestored. The size of the look-up tables is reduced by storing only those multiplication results which cannot be obtained by a shifting operation performed on the other pre-stored multiplication results, the input sample data, or the delayed sample data. Thereby, the size of the look-up tables can be compressed significantly such that an implementation of large digital filters into FPGAs is possible (see Schier Abstract).

It is submitted that Bhandal and Schier do not teach or suggest a method for performing multiplication on a field programmable gate array that includes generating a product by multiplying a first plurality of bits from a first number and a first plurality of bits from a second number using a digital signal processor (DSP) configured to perform multiplication on a fewer number of bits then those forming the first and second numbers, retrieving a stored value designated as a product of a second plurality of bits from the first number and a second plurality of bits from the second number from a memory, scaling the product with respect to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number and scaling the stored value with respect to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number, and summing a scaled product and a scaled stored value to generate a value representing a product of the first number and the second number, wherein the first number and the second number each have a number of bits equal to or greater than a total of the first and second plurality of bits.

The Office acknowledges that Bhandal does not disclose retrieving a stored value designated as a product of a second plurality of bits from a first number and a second plurality of bits from a second number from memory.

With respect to Claims 1 and 21, the Office has stated in part that

> Bhandal et al. fail to disclose the multiplier is on a field programmable gate array and the second product is retrieved from a memory. However, Schier et al. disclose in Figures 1-4 the multiplier is on a field programmable gate array (e.g. abstract) and the second product is retrieved from a memory (e.g. any intermediate product from the LUT in Figures 1-4 as b1x).
>
> Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the multiplier is on a field programmable gate array and the second product is retrieved from a memory as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3, lines 9-11 and col. 4, lines 9-12).

(4/1/2008 Office Action, p. 4 and 11).

Applicants submit, however, that Schier teaches away from combining a DSP biased multiplier such as that described in Bhandal with an FPGA biased multiplier such as that described in Schier. Firstly, Bhandal discloses a multiplier having paired multipliers 800 and 801 coupled to shifters 811 and 810 respectively and an adder 820 to perform multiplication. Shifters 811 and 810 are each configured to perform 16x16 multiplication of portions of two 32 bit data word (see Bhandal column 2, lines 53-61 and column 7, lines 31-43, and Figure 8). By disclosing a multiplier that generates a first product by multiplying a first 16 bits of a first data word with a first 16 bits of a second data word with multiplier 801 and that generates a second product by multiplying a second 16 bits of a second data word with a second 16 bits of a second data word with multiplier 800, Bhandal clearly uses a multiplier that is configured to perform multiplication on all the number of bits used for forming the first and second numbers being

multiplied, and is not using a multiplier that is configured to perform multiplication on a fewer number of bits than those forming the first and second numbers.

Applicants respectfully disagree with the Office that "it would have been obvious to a person having ordinary skill in the art at the time of the invention is made to add ... the second product ... retrieved from a memory as seen in Schier... because it would ... improve system performance." In the example disclosed in Bhandal, the number of bits of the numbers being multiplied, 32, match the configuration of the number of bits multiplied by multipliers 800 and 801, 32. Thus, there is no need or motivation to add a further product from memory. Furthermore, because there is a match, there would be no improvement in system performance. In fact, by requiring a stored product to be added, the multiplier's performance would worsen not improve.

Secondly, Schier discloses a digital filter that includes a look-up table (LUT) based multiplier 2 (see Figure 1). The digital filter disclosed in Schier is implemented on a field programmable gate array (FPGA) (see Schier column 4, lines 3-12 and column 9, lines 6-19). The LUT based multiplier 2 disclosed in Schier is not implemented on a DSP. Schier points out that digital filters have distinct architectures used for implementation and that these architectures fall into one of three categories: digital signal processors, application specific integrated circuits, *or* field programmable gate arrays. Schier specifically states

> The performance of the digital filter depends on the architecture used for implementation, i.e. DSP (Digital Signal Processor), ASIC (Application Specific Integrated Circuit) *or* FPGA (Field Programmable Gate Array).

(Schier column 1, lines 28-31) (Emphasis Added).

Clearly, Schier intends for a digital filter to have an architecture from only one of the three groups listed. Thus not only is the digital filter described and illustrated in Schier not a DSP, Schier teaches away from combining the DSP based architecture of Bhandal with the FPGA based architecture of the digital filter described in Schier.

The Office states in part that

> Nowhere in the specification of the secondary reference explicitly states that the FPGA and second product is retrieved from a memory CANNOT combine with other configurations, particularly the configuration cited in the primary reference.

(7/16/2008 Advisory Action, p. 2).

Applicants respectfully requests that the Office explain why then does Schier state that a digital filter would have an architecture from a DSP, ASIC, ***or*** a FPGA.

Thirdly, Applicants submit that "the intermediate product from the LUT in Figures 1-4" of Schier cannot be arbitrarily used as "the second product" as the Office suggests on page 4 of the Office Action mailed 4/1/2008. The Office states that both the product generated by the DSP and the stored value from memory are scaled in Bhandal by the shifters 810 and 811 illustrated in Figure 8.

> Re claim 1, Bhandal et al. disclose in Figures 1-22 a method for performing multiplication (e.g. abstract and Figure 8 as general architecture of multiplier), comprising: generating a product by multiplying a first plurality of bits from a first number and a second plurality of bits from a second number (e.g. Figure 11B wherein SRC1_L as B is multiplying with SRC2_L as D by B*D) using a digital signal processor (DSP) configured to perform multiplication on a fewer number of bits then those forming the first and second numbers (e.g. by multiplier 800 in Figure 8 wherein the multiplier 800 performs 16 bits multiplication of 32 bits operands); a product of a second plurality of bits from the first number and a second plurality of bits from the second number (e.g. Figure 11 wherein SRC1_H as A is multiplying with SRC2_H as C by A*C); scaling the product with respect to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number (e.g. by shifter 810 in Figure 8) and scaling the stored value with respect to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number (e.g. by shifter 811 in Figure 8); and summing a scaled product and a sealed (sic) stored value to generate a value representing a product of the first number and the second number (e.g. output of adder 820 in Figure 8 and Figure 11B), wherein the first number and the second number each have a number of bits equal to or greater than a total of the first and second plurality of bits (e.g. Figure 11B wherein each of input operands consist of 32 bits and each of input multiplied operand is 16 bits).

(4/1/2008 Office Action, pp. 3-4) (Emphasis Added).

Applicants submit that the Schier discloses a filter with a LUT based multiplier where additional shifting operations are not performed after multiplications. Schier specifically states

> Moreover, since the input sample data is **not** divided into its bit positions, an additional shifting operation is **not** required after the multiplications and a low latency is introduced.

(Schier column 4, lines 3-6) (Emphasis Added).

Thus, clearly Schier discloses a product that is of a type that does not require shifting. Applicants submit that Schier does not permit the shifting which the Office is requiring for the "stored value" by shifter 811 in Figure 8 of Bhandal, because the shifting would render the result incorrect and would introduce additional latency as Schier avoids as stated in column 4, lines 3-6.

In the Advisory Action mailed 7/16/2008, the Office states in part that

> The secondary reference does not need to show every limitation cited in the claims such as additional shifting operations after the multiplications in FPGA. In generally (sic), the primary reference shows most of elements in the claimed invention except the FPGA and the second product is retrieved from a memory.

(7/16/2008 Advisory Action, p. 2) (Emphasis Added).

Applicants respectfully submit that the Office has misunderstood Applicants position. Applicants are not stating that both Bhandal and Schier are required to disclose a same limitation in a 35 U.S.C. §103 rejection. Applicants are stating that Schier is disclosing a multiplier having certain stated characteristics for an intended purpose (a product that is not to be shifted) and that by combining Bhandal with Schier in the manner the Office suggests, the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose. Applicants submit that when this is the case, there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900 (Fed. Cir. 1984). Applicants further submit

that it is improper to combine references where the references teach away from their combination. In re Grasselli, 713 731, 743 (Fed. Cir. 1983).

In contrast, claim 1 states

> A method for performing multiplication of a first number with a second number on a field programmable gate array without utilizing a digital signal processor (DSP) capable of multiplying a number of bits forming the first and second numbers, comprising:
> generating a product by multiplying a first plurality of bits from the first number and a first plurality of bits from the second number using a DSP configured to perform multiplication on a fewer number of bits then those forming the first and second numbers;
> retrieving a stored value designated as a product of a second plurality of bits from the first number and a second plurality of bits from the second number from a memory;
> scaling the product with respect to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number and scaling the stored value with respect to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number; and
> summing a scaled product and a scaled stored value to generate a value representing a product of the first number and the second number, wherein the first number and the second number each have a number of bits equal to or greater than a total of the first and second plurality of bits.

(Claim 1, as Amended) (Emphasis Added).

Claims 11, 17, 21, and 22 include similar limitations.

Given that claims 3, and 5-10 depend from claim 1, claims 12-16 depend from claim 11, and claims 18-20 depend from claim 17, it is likewise submitted that claims 3, 5-10, 12-16, and 18-20 are also patentable under 35 U.S.C. §103(a) over Bhandal and Schier.

It is further submitted that Bhandal and Schier do not teach or suggest a multiplier that includes a digital signal processor (DSP) configured to perform multiplication on a first plurality of bits from a first number and a first plurality of bits from a second number, a memory that stores products resulting from multiplication of a second plurality of bits from the first number and a second plurality of bits from the second number, and an adder that sums a scaled output of

the DSP and a scaled output of the memory to output a value representing a product of the first and second number where the first and second number each have more than the first plurality of bits, wherein the DSP is only configurable to support multiplication of a number of bits equal to or less than the first plurality of bits, wherein the DSP, the memory, and the adder reside on a field programmable gate array.

The Office states in part that

> The examiner respectfully submits that Figures 1-4 and abstract of the secondary reference clearly disclose the above missing feature as FPGA wherein the FPGA includes the DSP for processing/filtering, the memory for storing, and the adder for adding.

(7/16/2008 Advisory Action, p. 2)

Applicants respectfully disagree. Schier discloses a digital filter that includes a look-up table (LUT) based multiplier 2 (see Figure 1). The digital filter disclosed in Schier is implemented on a field programmable gate array (FPGA) (see Schier column 4, lines 3-12 and column 9, lines 6-19). Schier points out that digital filters have distinct architectures used for implementation and that these architectures fall into one of three categories: digital signal processors, application specific integrated circuits, ***or*** field programmable gate arrays. Schier does not disclose a DSP on a field programmable gate array. In fact, Schier specifically states in part

> The performance of the digital filter depends on the architecture used for implementation, i.e. DSP (Digital Signal Processor), ASIC (Application Specific Integrated Circuit) ***or*** FPGA (Field Programmable Gate Array).

(Schier column 1, lines 28-31) (Emphasis Added).

Clearly, Schier intends for a digital filter to have an architecture from only one of the three groups listed and thus teaches away from combining the DSP based architecture of Bhandal with the FPGA based architecture of the digital filter described in Schier.

The Office cites the Abstract and Figures 1-4 of Schier as support that "the DSP, the memory, and the adder reside on a field programmable gate array". However, the Abstract of Schier makes absolutely no mention of a DSP on a field programmable gate array. Furthermore, the only reference to a DSP in the entire Schier patent is made to distinguish a DSP architecture from an FPGA architecture, not to describe having a DSP reside on an FPGA (see Schier column 1, lines 28-31). Figures 1-4 is also absent of a DSP on an FPGA. Applicants respectfully request that the Office clarify where specifically in the cited reference it believes it discloses a DSP on an FPGA.

In contrast, claim 18 states

> The multiplier of Claim 17, wherein the DSP, the memory, and the adder reside on a field programmable gate array.

(Claim 18) (Emphasis Added).

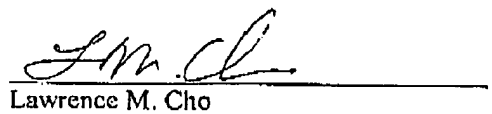
In view of the arguments set forth herein, it is respectfully submitted that the applicable rejections and have been overcome. Accordingly, it is respectfully submitted that claims 1, 3, and 5-22 should be found to be in condition for allowance.

The Examiner is invited to telephone Applicants' attorney (217-377-2500) to facilitate prosecution of this application.

If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,

Dated: September 1, 2008



Lawrence M. Cho
Attorney for Applicants
Registration No. 39,942

P.O. Box 2144
Champaign, IL 61825
(217) 377-2500